Abhinav Gorthy

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Education

- **University of Cincinnati** — Cincinnati, OH
  Ph.D. in Electrical Engineering — Aug 2025 - Present
  Coursework: VLSI Design, VLSI Test and Low Power Design, VLSI Design Automation, Computer Architecture, Nanoelectric Devices, Intelligent Systems, Trust in Digital Hardware

- **University of Cincinnati** — Cincinnati, OH
  Master of Science in Electrical Engineering (GPA: 3.4/4.0) — Aug 2023 - July 2025
  MS Thesis: A Comparative Study of HfO_2/MgO Charge Trap Flash Memory and OHP/DNA RRAMs

- **Jawaharlal Nehru Technological University** — Hyderabad, India
  Bachelor of Technology in Electronics and Communications Engg. (GPA: 8.4/10) — Aug 2019 - Jun 2025

Skills

- **Programming and Scripting Languages**: Python, C, C++, Verilog HDL, VHDL, TCL
- **EDA Tools**: Synopsys HSPICE, Design Compiler, ICC II, TetraMAX, TCAD Sentaurus, Cadence Virtuoso, Xcelium, Genus, Innovus, OpenLane
- **Cleanroom Experience**: Wafer cleaning, Oxidation, RIE, PVD, Photolithography, Wet Etching
- **Equipment Expertise**: Keithley 4200-SCS Parameter Analyzer, Cascade Probe Station, Lakeshore Cryotronics Cryogenic Probe Station, AJA Orion Sputtering System, March CS-1701 RIE, Nanonex NX-2600 Lithography
- **Technical Knowledge**: Analog IC Design & Verification, Custom Layout Design (Full-Custom & Semi-Custom), Memory Circuit Design (SRAM, DRAM, NAND), RTL-to-GDSII Flow, Low-Power Design Techniques

Professional Experience

Graduate Research Assistant - MIND Lab, UC (Advisor: Dr. Rashmi Jha) — **Oct 2023 - Present**

Device Characterization and Reliability Analysis

- Conducted electrical characterization (C–V, I–V, frequency-dependent analysis, endurance, and retention) of charge trap flash memory and RRAM devices using Keithley 4200A-SCS Semiconductor Parameter Analyzer.
- Performed reliability and failure analysis testing protocols, including temperature-based retention, BTI and TDDB using a Lakeshore Cryogenic Probe Station.
- Performed heavy ion radiation experiments on TaOx RRAM devices and involved in Focused Ion Beam (FIB) cross-section preparation, TEM/EDS analysis to assess structural degradation.
- Investigated conduction mechanisms by fitting experimental results to physics-based equations and executed statistical data analysis using Python.

Device Fabrication

- Implemented Design of Experiments (DoE) to optimize TaO_x RRAM stacks with Cu active electrodes, achieving high $R_{ON}/R_{OFF} > 10^3$ at low operating voltages (< 1 V) with multi-state switching capability.
- Performed photolithography for top electrodes on 4-inch Si wafers (device areas: 30–150 μm^2) with 97% yield and developed wet etching recipes for metals and insulators.
- Collaborated with Penn State University to fabricate biocompatible RRAMs using OHP and DNA layers, advancing towards CMOS-compatible integration.

Device Modeling and Circuit Simulations

- Simulated two-terminal Charge Trap Flash memory stack (W/MgO/HfO_2/MgO/p-Si) in TCAD Sentaurus using trapping and tunneling models and analyzed capacitance shifts and evaluated endurance and retention
- Developed sweep-based and pulse-based RRAM models in Verilog-A from experimental data.
- Designed a 4×4 1T–1R RRAM crossbar in Cadence Virtuoso with integrated selection circuitry and voltage-latched sense amplifiers.
- Working towards tape-out with heterogeneous integration of bio-compatible RRAMs and custom readout circuits.

Projects

Design and Layout of 64 Bit SRAM (Tools: Cadence Virtuoso; PDK : gpdk45nm) **Oct 2024**

- Designed a 64 bit SRAM array (8x8) using optimized 6T bitcells and integrated custom row/column decoders and sense amplifiers.
- Validated read/write operations through transient and steady-state simulations in ADE Explorer.
- Developed entire layout in Layout XL and ensured design integrity with LVS, DRC checks, and parasitic extraction using ASSURA and QUANTUS

RTL-to-GDSII Implementation of a CPU Macro (Tools: OpenLane EDA; PDK: Skywater 130nm) **June 2024**

- Synthesized Verilog code for PICORV32A (VSD CPU Macro) and completed its physical design using OpenLane TCL scripts and developed design constraints.
- Created a custom cell, extracted a SPICE file to measure input/output slew and delay, and generated a LEF file to integrate the cell into the design flow.
- Achieved positive setup & hold slack in timing analysis through ECO strategies.

Development of VLSI Partitioning, Placement, and Routing Tools (Tools: Visual Studio Code) **Feb 2024**

- Developed a C++ tool for two-way bipartitioning using the Kernighan-Lin heuristic, tested on netlists up to 40,000 cells and 4,000,000 nets.
- Implemented placement and routing algorithms based on force-directed placement and channel routing, validated on benchmarks with up to 2,000 cells and nets.

Square Root Machine Synthesis with DFT (Tools: Design Compiler, TetraMAX, ModelSim) **March 2024**

- Synthesized a gate-level netlist of a square root machine using Verilog with SAED 90nm PDK and inserted scan chains into the design using TCL
- Generated test patterns and extracted RTL switching activity data using ModelSim to produce a VCD (Value Change Dump) file, converting it to SAIF (Switching Activity Interchange Format) for power estimation.
- Achieved 99.08% fault coverage using TetraMAX, optimizing timing, area, and power metrics pre and post-scan insertion.

Bit-Sliced 4-Bit First in First Out (FIFO) (Tools: ModelSim, HSPICE, IRSIM, Magic VLSI) **Nov 2023**

- Designed a tape-out-ready 4-bit FIFO chip (60-bit slices) using ON C5 0.5µm n-well CMOS process, clocked at 100 MHz for efficient push/pop operations.
- Developed VHDL code and test bench; included standard cell delays for practical waveform simulation.
- Executed an optimized custom layout using M1, M2 metal interconnects with zero DRC errors; performed LVS check by extracting to SPICE and calculated propagation delays.

Publications

- Keremane, K.S., **Gorthy, A.**, Zheng, L., Ravi, C.C., Wu, H., Yennawar, N.H., Priya, S., Jha, R., Poudel, B.," Molecularly Engineered Highly Stable Memristors with Ultra-Low Operational Voltage: Integrating Synthetic DNA with Quasi-2D Perovskites", *Nature Materials*, manuscript under review.
- **A. Gorthy**, V. K. Gogi, R. Srinivasan, J. Mayersky, K. Leedy, and R. Jha, "Thickness Dependent Analysis of Ultra-Thin MgO Tunneling and Blocking Layers in HfO2 Charge Trap Flash Memory", *Journal of Applied Physics*, manuscript under preparation.
- S. Gollapudi*, **A. Gorthy***, V. K. Gogi, R. Srinivasan, and R. Jha, "Stability Study of BEOL-Compatible Forming-Free TaO_x RRAM Devices Under Extreme Temperature and Radiation Conditions", *IEEE Access*, manuscript under preparation.

Patents

- IoT-Based Modern Food Service System (Indian Patent Application Number - 202341060583)
- The Automated Titrator (Indian Patent Application Number - 202141061676)